IN THE SPECIFICATION:

Please amend the appropriate paragraphs of specification in accordance with proposed changes as outlined hereinbelow:

Please amend the second paragraph on page 1 as follows:

There has been proposed a technique to reduce the number of pins through common use of the signal input/output pin for test and the signal input/output pin for ~~usual~~ normal operation in a semiconductor integrated circuit mounting a test circuit. Moreover, in recent years, an LSI comprising the analog and digital sections, in which an analog circuit and a digital circuit are mounted on the same semiconductor chip, has also ~~be~~ been proposed in response to further improvement in packing density of LSI.

Please amend the last paragraph beginning on page 1 and ending on page 2 as follows:

In such LSI comprising the analog and digital circuits, when it is required to use in common the signal input/output pin for testing and the signal input/output pin for ~~usual~~ normal operation, the input/output pin for testing corresponding to the test circuit of the digital section and the input/output pin for testing corresponding to the test circuit of analog section have been provided individually in order to prevent deterioration ~~of~~ in accuracy due to ~~the leak of~~ noise leakage to the analog section from the test circuit of the digital section because the analog circuit requires a higher degree of accuracy. Namely, it has been avoided to use in common the input/output pin for testing corresponding to the test circuit of the digital section and the input/output pin for usual operation of the analog section.

Please amend the first paragraph under "Summary of the Invention" on page 2 as follows:

However, when the number of pins required for ~~usual~~ normal operation increases corresponding to progress in the packing density of LSIs, it has been required to use the input/output pin for ~~usual~~ normal operation of the analog section as the input/output pin for testing corresponding to the test circuit because of the necessity ~~of~~ in reducing ~~reduction~~ in ~~size of~~ package size through a reduction in the total number of pins.

Please amend the second paragraph under "Summary of the Invention" on page 2 as follows:

Therefore, the inventors of the present invention have investigated using ~~to use~~ in common the input/output pin for testing corresponding to the test circuit of the digital section and the input/output pin for ~~usual~~ normal operation of the analog section. At the beginning, the inventors have thought, on the occasion of using the pin usually used as the input/output of the analog section as the input/output pin for testing corresponding to the test circuit of the digital section, there is no influence on the analog section from the digital section, if the test circuit is turned OFF in the ~~usual~~ normal operation mode because there is no exchange of signals between the analog input/output terminal and digital section.

Please amend the first full paragraph on page 3 as follows:

However, as a result of detailed investigations, it has been found that if the test circuit is turned OFF in the ~~usual~~ normal operation mode, a noise generated in the digital section is transferred through the signal path up to the analog input/output pin connected with the test circuit from the test circuit of the digital section, resulting in adverse effects on the analog circuit.

Please amend the second full paragraph on page 3 as follows:

It is therefore an object of the present invention to eliminate the adverse effect of noise, on a semiconductor integrated circuit comprising the analog and digital sections, that is generated in the digital section and transferred to the analog circuit through the signal path extended from the test circuit of the digital section up to the analog input/output pin connected with such a test circuit even in the case that the input/output pin for testing corresponding to the test circuit of the digital section is also used in common as the input/output pin for ~~usual~~ normal operation of the analog section.

Please amend the fourth paragraph on page 4 as follows:

According to the means explained above, when the external terminal for common use is connected to the analog circuit, the wiring is disconnected from the digital circuit and is connected between the external terminal, and the digital circuit is fixed to the predetermined voltage. Therefore, noise generated in the digital circuit and noise leaked to the wiring from the peripheral circuits thereof are absorbed. Thereby, even when the external terminal is used in common with the analog circuit and digital circuit, transfer of noise to the analog circuit from the digital circuit can be prevented.

Please amend the second full paragraph on page 5 as follows:

Moreover, a voltage fixing mans for fixing the relevant wiring to the predetermined voltage under the condition that the relevant selection switch is shut off is connected respectively to the side nearer to the digital circuit than the selection switch of the wiring connecting between the external terminal and the digital circuit and to the side nearer to the selection switch. Thereby, if the eternal terminal is isolated from the digital circuit and thereby the wiring ~~connected~~ connecting these elements becomes longer, the voltage of the wiring can be fixed respectively at both ends of wiring with the voltage fixing means and accordingly the noise generated in the digital circuit and noise leaked to the wiring from the peripheral area c an be absorbed effectively and thereby influence of noise on the analog circuit can be lowered.

Please amend the first full paragraph on page 7 as follows:

Moreover, the voltage fixing means is formed on the surface of the semiconductor region sandwiched between two insulated separation bands in which the wiring connecting between the selection switch and digital circuit is formed. Thereby, the amount of noise appearing on the voltage fixing means and resulting from the peripheral circuits can be reduced and as a result, noise to be transferred to the analog circuit can also be reduced.

Please amend the second full paragraph on page 5 as follows:

In addition, the external terminal of the analog circuit is structured for common use as the terminal for inputting and outputting the signals of the test circuit of the digital circuit. Since the test circuit of the digital circuit is not operated during the ~~usual~~ normal operation of the analog circuit, the terminals can be used in common and any influence is applied to the usual operation because it is not required to select the terminals for ~~usual~~ normal operation.

Please amend the last paragraph beginning at the bottom of page 7 and continuing to the top of page 9 as follows:

Moreover, the other invention of the present specification is a semiconductor integrated circuit for processing various signals comprising an oscillation control circuit for generating [[a]] control voltages of a first oscillation circuit for generating a first oscillation signal and of a second oscillation circuit for generating a second oscillation signal, an amplifying circuit for amplifying a receiving signal, a first mixer circuit for combining the

amplified signal and the first oscillation signal to convert the frequency, a receiving analog circuit including a demodulation circuit for demodulating the signal frequency-converted in the first mixer circuit, a modulation circuit for modulating a transmitting signal, a transmitting analog circuit including a second mixer circuit for combining the modulated signal and the second oscillation signal to convert the frequency, a control digital circuit for controlling the receiving analog circuit and transmitting analog circuit and a test circuit for outputting a signal from the control digital circuit, whereby at least an external terminal for inputting an analog input signal to the transmitting analog circuit or outputting an analog output signal from the transmitting analog circuit is used in common as the external terminal for outputting the signal from the test circuit, the selection switches are respectively provided in the course of the wiring connecting the external terminal and analog circuit and the wiring connecting the external terminal and the digital circuit, and a voltage fixing mans for fixing the relevant wiring to the predetermined voltage under the condition that the relevant selection switch is in the shut-off condition is connected in the side nearer to the digital circuit than the selection switch of the wiring connecting the external terminal and digital circuit.

Please amend the fifth paragraph on page 10 as follows:

Fig. 6 is a cross-sectional view showing an example of the structure of a MOSFET to form a digital circuit and a detection switch and a noise absorbing switch of the embodiment of Fig. 1.

Please amend the second paragraph on page 11 as follows:

In Fig. 1, 100 designates a semiconductor chip; 110, a digital section where the digital circuit is provided; 120, an analog section where the analog circuit is provided; and 130, a mode selection control circuit for switching the operation mode in the chip depending on a mode setting signal supplied from an external circuit. The digital section 110 is provided with a digital circuit 111 and test circuit 112 for testing this digital circuit. Moreover, 141 designates an analog input/output pin for inputting a signal to the analog section 120 and outputting a signal from the analog section during the ~~usual~~ normal operation; 142, a mode setting pin for inputting a mode setting signal MODE to the mode selection control circuit 130, and 143, a signal input/output pin during the usual operation of the digital circuit 111.

Please amend the third paragraph beginning on page 11 as follows:

The digital section 110 and analog section 120 are respectively structured to be operated with different power supply systems (including the case where the level is same). ~~In more practical~~ More practically, the digital section 110 is connected with the power supply wiring extended from the power supply terminal 151 for receiving the power supply voltage Vcc1 supplied from the external circuit of the chip, while the analog section 120 is structured to be connected to the wiring extended from the power supply terminal 152 for receiving the power supply voltage Vcc2 supplied from the external circuit of the chip and to receive the power supply from the individual power supply terminals.

Please amend the first full paragraph on page 12 as follows:

As explained above, it can be prevented by providing individual power supply terminals and power supply wirings for the digital section 110 and analog section 120 that variations in the ~~of~~ power supply diffuses to the analog section 120 due to the operation of the digital section 110 to lower the accuracy. Moreover, it is preferable that the power supply terminals 151, 152 are connected to different lead terminals provided to a package. Moreover, the ground lines and external terminals for supplying the ground potential are also individually formed for the digital section 110 and analog section 120.

Please amend the last paragraph beginning on page 12 as follows:

In the semiconductor integrated circuit of this embodiment, a signal line 160 for outputting the operating condition in the test circuit 112 to the external side from the analog input/output pin 141 is provided between the analog input/output pin 141 and test circuit of the digital section 110. Moreover, selection switches 171, 172 for controlling ON and OFF the transmission of signals are respectively provided in the side nearer to the analog input/output pin 141 of the signal line 160 and between the analog input/output pin 141 and analog section 120. These selection switches 171, 172 are controlled to ON and OFF conditions. Namely, the selection switch 171 is turned ON and the switch 172 is turned OFF during the test with the test circuit of the digital section with the control signal SC from the mode selection control circuit 130 and the signal /SC converted with an inverter 131, while the selection switch 171 is turned OFF and the switch 172 is turned ON during the usual operation.

Please amend the first paragraph beginning on page 13 and ending on page 14 as follows:

Moreover, in this embodiment, the switches 173, 174 are also provided respectively to the selection switch 171 side of the signal line 160 and at the area near the test circuit 112 of the digital section in view of absorbing noise[[s]] by fixing, to the constant voltage such as the ground potential, the voltage of the signal line 160. These noise absorbing switches 173, 174 are turned OFF during the test with the test circuit of the digital section with the control signal from the mode selection control circuit 130, while [[are]] being turned ON during the ~~usual~~ normal operation. The ground lines as the constant voltage lines connected with the noise absorbing switches 173, 174 are respectively defined as follows. Namely, the noise absorbing switch 173 is used as the ground line GND2 in the analog circuit side, while the switch 174 as the ground line GND1 in the digital circuit side.

Please amend the first full paragraph on page 15 as follows:

In above explanation, the analog input/output pin 141 which is used in common also with the test circuit 112 of the digital section 110 is used to output the operating condition of the test circuit 112, but when the analog input/output pin 141 is also used in common as the pin for inputting the test signal to the test circuit 112 of the digital section 110, it can also be prevented that noise from the digital section 110 is transferred to the analog section 120 via the signal line 160 because the noise absorbing switches 173, 174 are provided and are then turned ON during the ~~usual~~ normal operation and noise appearing from the peripheral circuits is transferred to the analog section 120 because the signal line 160 works as an antenna.

Please amend the second full paragraph on page 16 as follows:

In Fig. 2, 210 designates a receiving circuit for amplifying and demodulating an input receiving signal; 220, a transmitting circuit for modulating a transmitting signal and converting the frequency thereof; 230A, 230B, oscillation circuits for generating local oscillation signals required for these receiving circuit 210 and transmitting circuit 220; and 240, a control circuit for controlling the receiving circuit 210 and transmitting circuit 220. In this embodiment, the receiving circuit 210 and transmitting circuit 220 are formed as the analog circuit and the control circuit 240 is formed as the digital circuit.

Please amend the last paragraph on page 16 as follows:

The receiving circuit 210 includes a low noise amplifying circuit (LNA) 211 for amplifying an input receiving signal, a mixer (MIX) 212 for direct down-conversion of the combined receiving signal amplified with LNA and the local oscillation signal from the

oscillation circuit 230A to the signal of base-band frequency (I/Q) and for demodulation of the signal and a programmable gain amplifier (PGA) 213 which can control the gain thereof by amplifying the down-converted receiving signal to the desired level.

Please amend the last paragraph on page 17 as follows:

The transmitting circuit 220 is formed of a modulator (I/Q MOD) 221 for modulating the signal inputted as the baseband signal (I/Q) converted from the audio signal in the baseband signal (I/Q) not shown and a mixer (U-MIX) 222 for up-conversion of the modulated signal up to the predetermined transmitting frequency by combining such modulated signal and the oscillation signal from the oscillating circuit 230B or the like. The mixer 222 may be an ordinary mixer circuit but can also be formed as a circuit which considers the oscillation signal supplied from the oscillating circuit 230B as the carrier and can output ~~in direct~~ directly such carrier with inclusion of the signal modulated in the modulator (I/Q MOD) 221.

Please amend the first paragraph on page 19 as follows:

In addition, the semiconductor integrated circuit for signal processing of this embodiment is individually provided with the power supply terminals (151, 152, ...) and the ground terminal respectively corresponding to the receiving circuit 210, transmitting circuit 220, oscillating circuit 230 and control circuit 240. Moreover, the oscillating circuit 230 is also provided with individual power supply terminals corresponding to the receiving synthesizer RF-SYN and transmitting synthesizer IF-SYN. Thereby, the power supply noise of the- oscillating circuit 230 and control circuit 240 is not easily transferred to the receiving circuit 210 and the transmitting circuit 220 as the analog circuit via the power supply line. From the point of view of reducing the power supply noise for the analog circuit, the power supply pin provided to the package may be used in common for the oscillating circuit 230 and control circuit 240, except for the power supply terminal of the chip (pad). Namely, the individual pads may be connected to the same power -supply pin with a bonding wire.

Please amend the second full paragraph on page 20 as follows:

Moreover, in the semiconductor integrated circuit for signal process of this embodiment, the signal line 160 for connecting the signal selection circuit 170 and the test circuit 112, of the digital circuit 111 [[is]] are formed in the narrower island region sandwiched between two guard band lines GBL1, GBL2 formed on the chip surface.

Please amend the last paragraph beginning on page 20 as follows:

Although not particularly restricted, in an example of Fig. 3, an input pin of the analog control signal for the transmitting circuit 220 from the baseband process circuit is used as the common pin 141 and this pin 141 is then connected with a differential amplifying circuit 180. In Fig. 3, 160 designates a signal line for testing connected to the test circuit 112 of the digital section; 171, a selection switch connected between the signal line 160 and common pin141; 172, a selection switch connected between the common pin 141 and the differential amplifying circuit 180 as the analog circuit; and 173, a noise absorbing switch connected between the signal line 160 and the ground point (ground line).

Please amend the last paragraph beginning on page 21 as follows:

The differential amplifying circuit 180 is formed [[of]] from a pair of MOSFETs Ql, Q2 for receiving respectively at the gate terminals, the differential control signals inputted to the common pins 141, 145 during the ~~usual~~ normal operation, constant current sources Il, 12 connected to the source terminal side of the MOSFETs Q1, Q2 a resistor RO connected between the source terminals of Q1, Q2 and drain resistors R1, R2 connected between the drain terminals of Ql, Q2 and the ground point. The input differential signal amplified with this differential amplifying circuit 180 is then supplied to the modulator (I/Q MOD) 221 and the mixer (U-MIX) 222 shown in the embodiment of Fig. 2 via a buffer amplifier 181.

Please amend the first full paragraph on page 22 as follows:

Fig. 4 shows a practical example of the test circuit 112 connected to the analog input/output pin 141 for testing in the semiconductor integrated circuit of the embodiment of Fig. 2.

Please amend the first paragraph on page 23 as follows:

As explained above, since the signal line 160 connecting the common analog input/output pin for test from the test circuit of the digital section is provided with switches 173, 174 in this embodiment, noise transferred to the analog section 120 from the digital section 110 via the signal line 160 can be absorbed. Here an LSI comprising the analog and digital sections provides ~~a fear for transfer~~ the possibility of transferring ~~of~~ noise to the analog section from the digital section via the substrate, but in this embodiment, such noise diffused from the substrate can be suppressed as much as possible through the employment of

a separation between the power supply line and power supply terminal explained above, a device structure called the SOI (Silicon On Insulator) explained hereafter and U-groove separation structure.

Please amend the first full paragraph on page 25 as follows:

Moreover, in this embodiment, two groove isolation bands 51, 52 reaching the lower insulation film 30 through the epitaxial layer 40 are formed in parallel and the signal lines 160 for connecting the test circuit 112 to the analog input/output pin via the insulation film such as the silicon oxide film are formed on the narrow island type epitaxial layer 40 surrounded by such U-groove isolation bands 51, 52. These U-groove isolation bands 51, 52 are extended, in Fig. 1, up to the area near the test circuit 112 from the selection switch 171. As explained above, formation at the upper part of the narrow island type epitaxial layer 40 sandwiched by two U-groove isolation bands 51, 52 in which the signal lines 160 are formed in parallel to connect the test circuit to the analog input/output pin can prevent transfer of noise to the analog circuit through the signal lines 160 due to voltage variations or the like generated when the elements forming the peripheral circuits operate.

Please amend the last paragraph beginning on page 27 as follows:

The noise appearing from the signal lines provided in the course of the selection switch is usually considered as a problem in the present invention is usually not so much considered as a problem because this noise level is comparatively lower than the noise diffused from a substrate, but the noise appearing from the signal lines 160 in this embodiment ~~gives~~ has a relatively large influence because the noise diffused from the substrate is reduced through employment of the SOI structure and U-groove isolation structure. Therefore, the present invention can be adapted effectively in such a case where the analog input/output pin is used in common with the digital circuit in the LSI comprising the analog and digital sections of the SOI structure.

Please amend the first full paragraph on page 28 as follows:

The present invention has been explained in practical based on the preferred embodiment thereof, but the present invention is not limited to the above embodiment and allows of course various changes and modifications within the scope of the invention but not departing from the claims thereof. For example, in the above embodiment, the SOI substrate is used as a semiconductor substrate but ~~the~~ a similar effect can also be achieved by adapting

the present invention even when an ordinary silicon substrate is used. Moreover, in the above embodiment, the analog input/output pin is used in common for the test circuit of the digital section, but the present invention can also be adapted to the case where the analog input/output pin is also used in common for ~~the~~ digital circuits other than the test circuit under the condition, for example, of [[use]] usage on [[the]] a time division basis.

Please amend the last paragraph beginning on page 28 as follows:

In the above explanation, the present invention has been adapted to the LSI for signal processing to be used in [[the]] radio communication systems ~~of the~~ for hand-held telephone sets of [[the]] direct conversion systems which is the application field as the background of the present invention[[,]]. However, ~~but~~ the present invention is not restricted thereto and can also be widely adapted to the LSI for signal processing to be used for [[the]] radio communication systems of [[the]] hand-held telephone sets of [[the]] super-heterodyne systems and a semiconductor integrated circuit comprising the analog and digital sections.

Please amend the last paragraph on page 29 as follows:

That is, according to the present invention, there is provided the effect, even when the input/output pin of the signal corresponding to the digital circuit and the input/output pin of analog circuit are used in common in the semiconductor integrated circuit comprising the analog and digital sections., that the bad influence on the analog circuit [[of]] by the noise generated in the digital circuit and transferred through the signal route extended up to the analog input/output pin connected with the digital circuit from this digital circuit can be eliminated.